Features of the Digital Block of a Hardware Simulator for MIMO Radio Channels

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***Abstract*—The aim of the French regional research project SIMPAA2, which continues the former national research SIMPAA project, is the realization of a hardware simulator of MIMO propagation channels for UMTS and WLAN applications. The simulator must reproduce the behavior of the radio propagation channel, thus making it possible to test "on table" the mobile radio equipments. The advantages are: low cost, short test duration, possibility to ensure the same test conditions in order to compare the performance of various equipments. Two digital architectures are proposed and analyzed depending on the different environment characteristics.**

I. INTRODUCTION

The UMTS (Universal Mobile Telecommunications System) and WLAN (Wireless Local Area Network) tele-communication systems of third generation and beyond are able to offer to general public high-rate multi-media services. MIMO (Multiple-Input Multiple-Output) systems make use of antenna arrays at both sides of a radio link to drastically improve the capacity over more traditional systems.

However, the transmitted electromagnetic waves interact with the propagation environment (indoor/outdoor). It is thus necessary to take into account the main propagation parameters during the design of the future communication systems. The optimal choice of the modulation, coding, etc. for these communication systems is based on a reliable model of the radio propagation channel. Moreover, after the realization of a communication system, its experimental performance can be evaluated by using a hardware radio channel simulator. A hardware simulator can also be used to compare the performance of various radio communication systems in a time-variant propagation channel in the same test conditions. On the market, there are some hardware channel simulators: Propsim [1], Smartsim [2], Spirent [3], but they are very expensive and therefore prohibitive for a communication laboratory.

This paper presents the design of the digital block of a hardware simulator for indoor/outdoor MIMO radio channels. Section II of the paper deals with the architecture of the digital block of the hardware simulator. This section is divided into two parts: General Characteristics and Digital Block describing the proposed architectures and several parameters useful to design the hardware simulator. Last, in Section III, the accuracy of the hardware digital block for both proposed architectures is presented. The prototyping platform and the first results are also described.

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II. HARDWARE SIMULATOR

A. General Characteristics

The simulator must reproduce the behavior of a MIMO propagation channel for indoor and outdoor environments. It must operate with RF signals (2 GHz for UMTS and 5 GHz for WLAN). In order to make adjacent channels interference tests for UMTS systems, it is useful to consider three successive channels with 5 MHz bandwidth. Therefore, the frequency bandwidths B are 15 MHz for UMTS and 20 MHz for WLAN.

Moreover, UMTS uses two operating modes: the TDD mode (Time Division Duplex) having the same frequency band for both uplink and downlink and the FDD mode (Frequency Division Duplex) having different frequency bands. In addition, depending on the strength of the transmitted signals, the simulator must be able to accept input signals with wide power range, between - 50 and 33 dBm, which implies a power control for the simulator inputs.

The design and realization of the RF block for UMTS systems were completed in the previous SIMPAA (SImulateur Matériel de Propagation pour Antennes Adaptatives) project [4]. The RF block will need some modifications required by WLAN specifications. The objectives of the actual regional project SIMPAA2 mainly concern the channel model block and the digital block of the MIMO simulator, as shown in Fig. 1 by the gray blocks.

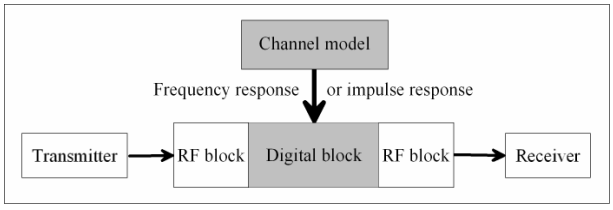

Figure 1. Block diagram of a one-way SISO channel.

The RF blocks and the channel model block have been described in [5]. For a one-way SISO (Single-Input Single-Output) channel, the first RF block realizes a frequency down-conversion. Its function is to obtain a real signal with a power spectrum within [0,B] frequency band to avoid complex computation and therefore to use less resources. The second RF block realizes the frequency up-conversion of the output signal.

The channel models used by the simulator are obtained from measurements by using a time domain MIMO channel sounder designed and realized at the IETR [6].

B. Digital Block

In order to have a suitable trade-off between complexity and latency, two solutions are necessary: a time domain approach with FIR filters for indoor environments and a frequency domain approach with FFT/IFT modules for outdoor environments.

For outdoor environments, as the impulse responses are longer, more samples are necessary to describe them. Therefore, computations are carried out in the frequency domain because FFT modules need less resources than FIR filters. The frequency domain architecture uses only one complex multiplication but needs one FFT module for each SISO channel and one IFT module. These modules increase the latency of the digital block.

On the other hand, for indoor environments, the FFT and IFT modules have too much latency, therefore it is more judicious to use FIR filters which carry out convolutions. Several real multipliers are used, their number depends on the length of the channel impulse response.

Fig. 2 describes the architecture of the digital block for both frequency domain and time domain.

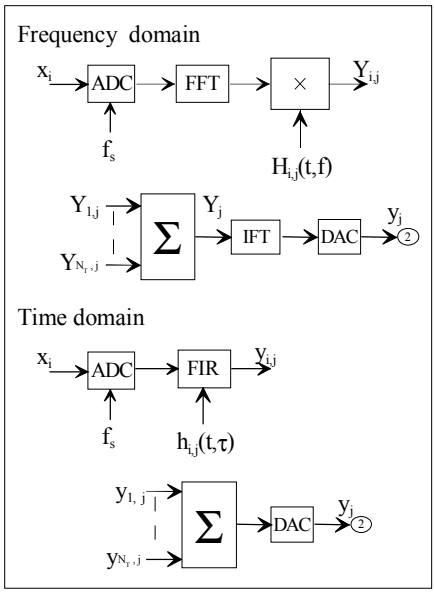

Figure 2. Digital block.

For an outdoor environment, the digital block operates in the frequency domain. The Fourier transform of the input signal, obtained at the output of the FFT block, is multiplied by the channel frequency response $H_{ij}(t,f)$. The signal $Y_j(t,f)$ is the sum of the contributions of each SISO channel. This signal is truncated depending on the number of bits of the input of the IFT block which gives the low-frequency output signal $y_j(t,\tau)$. After the D/A converter, the resulting signal represents the input of the up-conversion RF unit.

For an indoor environment, the digital block operates in the time domain. The FIR filter computes the convolution product between the sampled input signal and the channel impulse response $h_{ij}(t,\tau)$. As for the frequency domain, the signal $y_j(t)$ of the j^{th} receive antenna is the sum of the SISO $y_{ij}(t,\tau)$ signals. Then, this sum must be truncated according to the number of bits of the D/A converter.

Based on Shannon theorem and the performance of the RF/IF filters, the sampling frequency f_s was chosen to be 40 MHz for UMTS systems and 50 MHz for WLAN systems. This choice allows a reasonable low sampling rate and avoids the aliasing problems.

According to the considered propagation environments, Table I summarizes some useful parameters.

TABLE I. SIMULATOR PARAMETERS

	Type	Cell Size	W_{teff}(µs)	N	W_t(µs)
UMTS	Rural	2-20 km	20	512	12.8
(B = 15 MHz)	Urban	0.4-2 km	3.7	128	3.2
(f_s = 40 MHz)	Indoor	20-400 m	0.7	28	0.7
WLAN	Office	40 m	0.39	20	0.4
(B = 20 MHz)	Indoor	50-150 m	0.73	37	0.74
(f_s = 50 MHz)	Outdoor	50-150 m	1.16	64	1.28

For these various environments, the length of the FIR filter or the FFT/IFT blocks is estimated by:

$$N_{eff} = \frac{W_{teff}}{T_s} = W_{teff}.f_s \qquad (1)$$

where W_{teff} is the width of the effective time window of the channel impulse response, i.e. the width of the time-interval where the impulse response can be considered not null [7] [8]. For outdoor environment, due to FFT/IFT blocks, N is the closest 2^n value of N_{eff}. The resulting $W_t = N.T_s$ is also given in Table I.

III. IMPLEMENTATION

A. Simulations

The adopted solution uses a prototyping platform based on 3 development boards (XtremeDSP Development Kit-IV for Virtex-4) from Xilinx [9], shown in Fig. 3 which will be installed in a computer, contrary to RF blocks placed in an external unit.

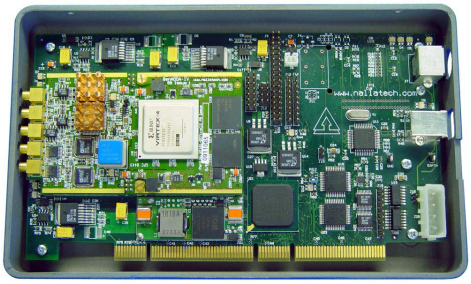

Figure 3. XtremeDSP Development board for Virtex-4.

This development board is built with a module containing the Virtex-4 SX35 programmable component which contains a large number of arithmetic blocks. Moreover, the XtremeDSP Development board provides a complete platform for high-performance signal processing applications. This board features

dual-channel high-performance ADCs (AD6645) and DACs (AD9772A) with 14-bit resolution, a support for external clock, programmable clocks, two banks of memory, interfacing via PCI or USB…

In order to determine the accuracy of the digital block, gaussian signals x(t) and h(t) are used. If $[-V_m,V_m]$ is the full scale of the converters, $x(t) = x_m \exp[-(t - m_x)^2/2\sigma_x^2]$, with $x_m = V_m/2$. The parameters of the test signals x(t) and h(t) are chosen in order to obtain $y(t) = y_m \exp[-(t - m_y)^2/2\sigma_y^2]$, with $y_m = V_m/2$, $m_y = W_t/2$ and $\sigma_y = m_y/4$.

The simulation of the architectures is made with Xilinx tools and the results are processed by MATLAB programs.

1) Frequency domain: The chain described in Fig. 4 is simulated with the parameters of Table I. In the worst case, 512-length Xilinx FFT/IFT blocks are used.

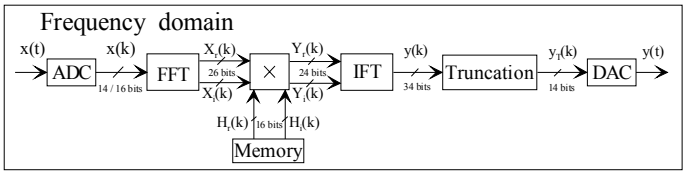

Figure 4. Frequency domain block diagram for a one-way SISO channel.

Due to the A/D converter, the real input signal x(t) is digitized on 14 bits, but 2 least significant bits are added in order to be accepted by the FFT block, which is equivalent to multiply the input signal by 4. The complex FFT output is multiplied by the channel frequency response, stored in a memory. This multiplier truncates its output on 24 bits (the maximum value accepted by the IFT block). The real output of the IFT block is truncated on 14 bits before to supply the D/A converter. The output signal is presented in Fig. 5. "XILINX" signal is the output of IFT block y(t) before truncation and "DAC" signal is the output with truncation on 14 bits.

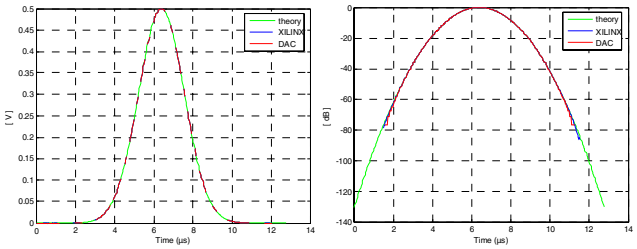

Figure 5. Frequency domain output signal in linear and log scale.

There is a very good agreement between the computed signals and the theory. The relative error and the signal to noise ratio (SNR) of the output signal are presented in Fig. 6.

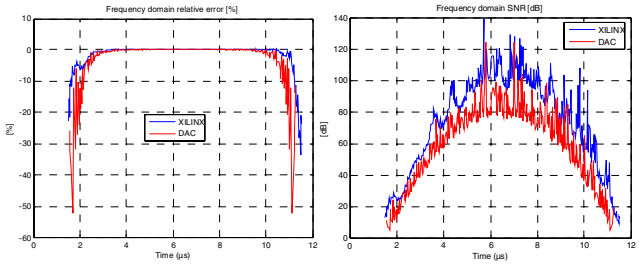

Figure 6. Frequency domain error and SNR for a one-way SISO channel.

Between 3 and 10 µs, the relative error is insignificant but it is greater for smaller values of the output signal.

The global values of the relative error and of the SNR of the output signal before and after final truncation are also computed by the following equations:

$$\varepsilon = \frac{||e||}{||y||} \times 100\ [\%],\quad SNR = 20\log_{10}\frac{||y||}{||e||}\ [\text{dB}] \qquad (2)$$

where y is the theoretical output signal, y_c is the computed signal (with or without truncation) and $e = y_c - y$.

If $x = [x_1, x_2, \ldots, x_N]$, then:

$$||\ x\ || = \sqrt{\frac{1}{N}\sum_{k=1}^{N} x_k^2} \qquad (3)$$

The results are $\varepsilon = 0.0058$ % and SNR = 84.79 dB without truncation. After 14 bits truncation, we obtain $\varepsilon = 0.0228$ % and SNR = 72.83 dB.

2) Time domain: According to Table I, the worst case for WLAN environments uses a FIR filter with a length of 64. For the time domain, we have developed our own FIR filter, instead of using Xilinx MAC FIR filter because this filter does not allow to reload the FIR filter coefficients. According to the resolution of the A/D and D/A converters, the input and the output of this filter have a 14-bit resolution. The coefficients of the channel impulse response have a 16-bit resolution. The 64 coefficients are stored in the 32-block memory via the PCI bus, each block storing two coefficients. These coefficients are read at 100 MHz and the input data at 50 MHz. Thus, each FIR multiplier is used twice during two cycles. The simulated time chain is described in Fig. 7.

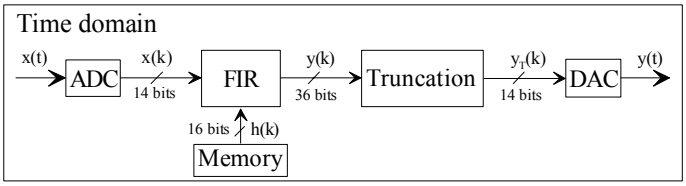

Figure 7. Time domain block diagram for a one-way SISO channel.

The output signal is presented in Fig. 8. Once again, one can remark an excellent agreement between Xilinx computed signals and the theoretical signal.

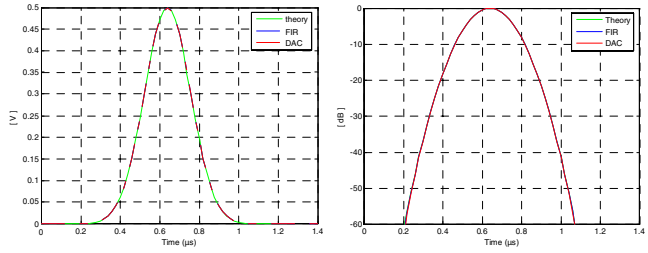

Figure 8. Time domain output signal in linear and log scale.

Fig. 9 shows the relative error and the SNR, computed for the output signal. Between 0.3 and 1 µs, the relative error is insignificant. Without truncation, the global relative error is

ε = 0.0105 % and SNR = 79.56 dB. After 14-bit truncation, we obtain ε = 0.0305 % and SNR = 70.32 dB.

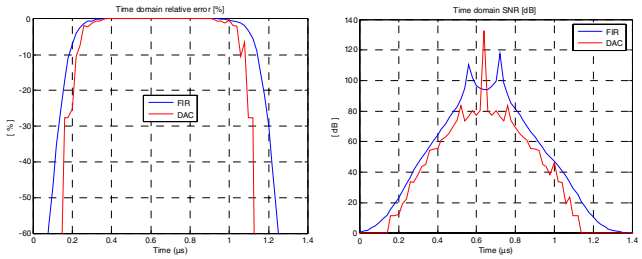

Figure 9. Time domain relative error and SNR for a one-way SISO channel.

B. *Synthesis*

With Xilinx ISE and Modelsim software, it is possible to synthesize each chain. Table II shows the device utilization for the frequency chain.

TABLE II. VIRTEX-4 SX35 UTILIZATION FOR FREQUENCY CHAIN

Number of Slices	8147 out of 15360	53 %
Number of logic LUTs	10444 out of 30720	22 %
Number of Block RAM	29 out of 192	15 %
Number of Flip Flops	12644 out of 30720	41 %
Number of DSP48s	78 out of 192	40 %

The frequency chain latency is measured between the time when the data enter the FFT block and the time when the result is provided at the IFT output. The latency is roughly 45 µs according to the Modelsim tools.

As a development board has 2 ADC and 2 DAC, it can be connected to only 2 down-conversion RF units and 2 up-conversion RF units. Therefore, 4 FIR filters are needed to simulate a one-way 2 x 2 MIMO radio channel. For the time domain, the V4-SX35 utilization summary is given in the Table III for 4 FIR 64 with their additional circuits used to dynamically reload the coefficients of the FIR filters (*i.e.*, the channel impulse response profiles). These coefficients are stored on the hard disk of the computer and read via the PCI bus. For 4 filters with 64 coefficients, the measured reloading time is 384,6 µs.

TABLE III. VIRTEX-4 SX35 UTILIZATION FOR 4 FIR 64

Number of Slices	7354 out of 15360	47 %
Number of logic LUTs	11318 out of 30720	36 %
Number of Block RAM	129 out of 192	67 %
Number of Flip Flops	9051 out of 30720	29 %
Number of DSP48s	128 out of 192	66 %

A FIR filter has 2 cycles of 32 multiplications and 5 addition cycles. One more cycle is necessary to add the results of each FIR. Thus, we have 8 cycles at 100 MHz, therefore 80 ns of latency for the digital block operation in the time domain. It is necessary to add approximately 38 ns of the ADC latency, and 17 ns of the DAC latency, according to their datasheets.

Moreover, for larger MIMO configurations, several boards connected together with point-to-point links must be used. Thus, the synchronization between these boards also needs one more clock cycle for both frequency and time domain architectures.

In summary, the digital block and the converters have a latency of 45 µs for the frequency domain and 135 ns for the time domain.

IV. CONCLUSION

SIMPAA2 project has two main objectives. The first objective concerns the design and the realization of the digital block of the hardware simulator. The second objective concerns the MIMO channel models which must supply the digital block.

After a comparative study, in order to reduce the complexity and the latency of the digital block, the output signal of the MIMO simulator is computed in the frequency domain for outdoor environments and in time domain for indoor environments. For both architectures, the simulation results obtained for a one-way SISO channel show an excellent accuracy of the output signal.

This work continues to complete the design of the architecture of the hardware simulator by maximization of its precision and minimization of the latency of the digital block. Therefore, an other architecture with FIR filter is being studied in order to reduce the latency of the frequency chain.

More measurement campaigns will be carried out with the MIMO channel sounder, realized by IETR, for various types of environments (indoor, outdoor, penetration) and for both UMTS and WLAN frequency bands. The final objective of these measurements is to obtain realistic and reliable impulse responses of the MIMO channel in order to supply the digital block of the hardware simulator.

Last, the digital block of the MIMO hardware simulator will be implemented as an electronic module. A Graphical User Interface (GUI) will be also developed to allow the user to configure the channel parameters: environment type, channel model, time window, mobile speed, etc.

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